(12) UK Patent Application (19) GB (11) 2 003 705 A

(21) Application No **7834266**
(22) Date of filing **23 Aug 1978**
(23) Claims filed **23 Aug 1978**
(30) Priority data
(31) **36101/77**
(32) **27 Aug 1977**
(33) **United Kingdom (GB)**
(43) Application published **14 Mar 1979**
(51) **INT CL$^2$ H04B 1/62 H04L 27/00**
(52) Domestic classification **H4P B6A B6Y C3 CD E9 F9**
(56) Documents cited
**GB 1506559**
**GB 1441767**
**GB 1363451**
**GB 1261771**
**GB 1262156**
**US 4039749**
**US 4017798**
(58) Field of Search **H4P**

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(54) **Spread spectrum data transmission**

(57) Spectrum spreading of a signal a(n) for a data transmission link is realised by providing the signal as a bipolar waveform and modulating it on a fast pseudorandom bipolar binary pulse train. The psuedo-random pulse train is generated at least in part in response to the data signal to provide the spread spectrum signal *b(n)*, Fig. 1. The signal a(n) is recovered in complementary manner, Fig. 2.

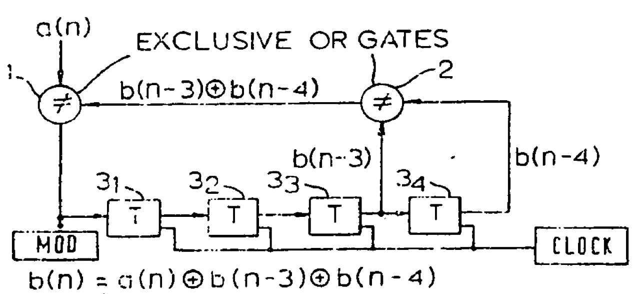


FIG. 1

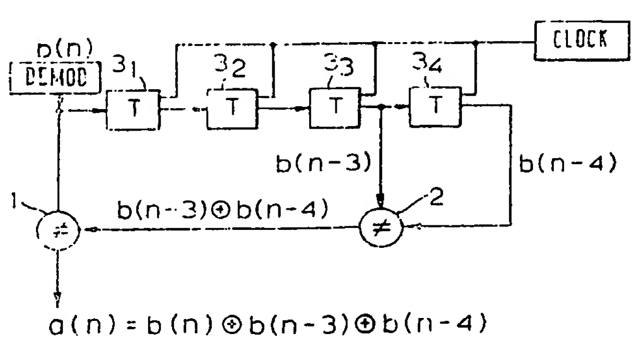


FIG. 2

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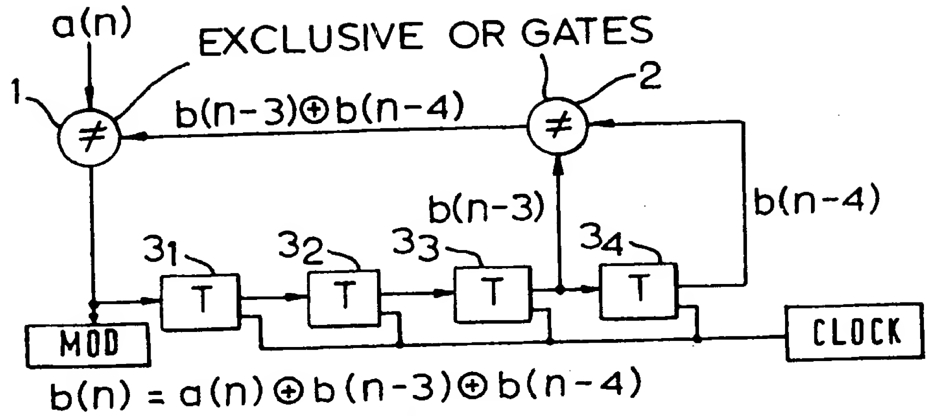
a(n)
EXCLUSIVE OR GATES
1
2
b(n-3)⊕b(n-4)
b(n-3)
b(n-4)
31
32
33
34
T
T
T
T
MOD
CLOCK
b(n) = a(n)⊕b(n-3)⊕b(n-4)

FIG. 1

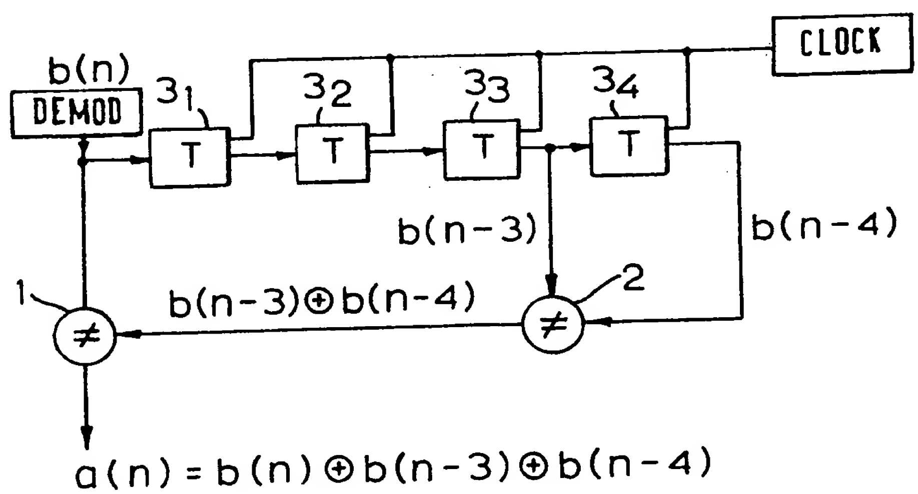
b(n)
DEMOD
CLOCK
31
32
33
34
T
T
T
T
b(n-3)
b(n-4)
1
2
b(n-3)⊕b(n-4)
a(n) = b(n)⊕b(n-3)⊕b(n-4)

FIG. 2

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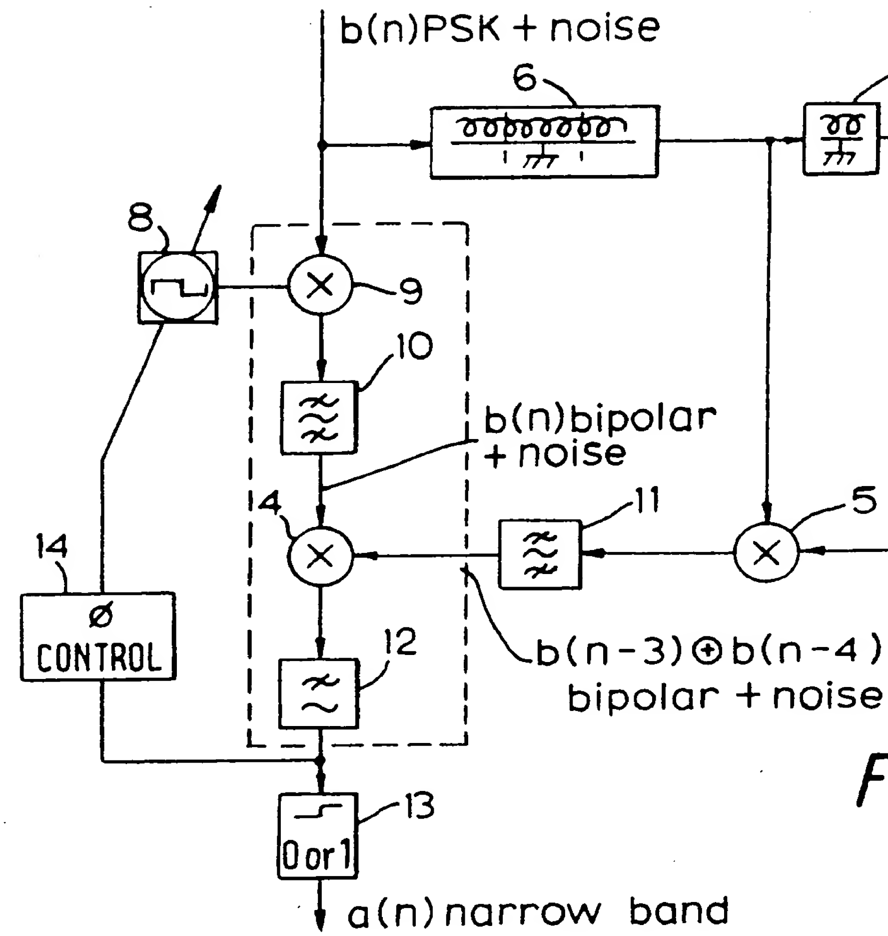


FIG. 3

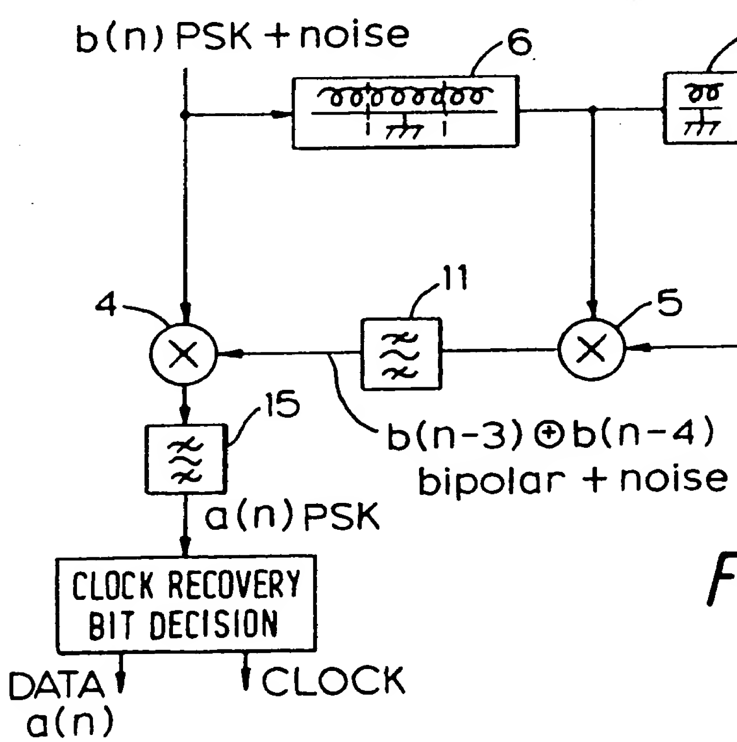


FIG. 4

SPECIFICATION

## Improvements in or relating to data transmission

The present invention relates to data transmission arrangements and is particularly related to data transmission over links, such as relatively long distance links, which may be subject to interference.

In known transmission arrangements, such as for example radio links between a number of individual units and one or more controlling or superivising units, the transmitted signals may be subject to noise as both narrow band and wide band interference.

To reduce the effects of such interference the signal may be arranged to occupy a much greater bandwidth than the base bandwidth of the data being conveyed. This technique, which may be called spectrum spreading, increases the probability of receiving some useful signal not excessively degraded by noise. If the noise is deliberately introduced, as jamming signals, the spectrum spreading forces the jammer to dissipate its power over the entire signal band. With some implementations of the technique, this reaction may be beneficial.

A well known technique of covering a wide bandwidth involves the use of wideband frequency modulated (f.m.) signals. When the amplitude probability distribution of the modulation waveform is well spread, as for audio or video analogue signals, the frequency spectrum of the modulated output is also evenly distributed. However, f.m. with a binary modulating waveform corresponds to shifting the instantaneous frequency from one value to another and back, known as frequency shift key (f.s.k.) coding. If the bit rate is much less than the frequency deviation (say half the difference between them), power tends to be concentrated about the two frequency values so that the signal is vulnerable to interference concentrated at those frequencies. The sparse wideband f.m. is unsatisfactory unless the gaps in the transmitted spectrum can be filled in, for example by an increase in bit rate or by random frequency agility.

An alternative application of f.m. is to sweep the instantaneous frequency over its full range in each data interval. The signal is received via a matched (compressive) filter. This is not entirely satisfactory since deliberately induced interference can readily be caused to simulate the modulation once it has been determined.

Because of these deficiencies it has become practice to phase reverse the binary data signal in a random manner to provide another binary waveform at a much higher effective bit rate. It is arranged so that the process may later be reversed by a circuit fed with the corresponding key. Conventionally this is done by adopting a bipolar ( + or − ) data waveform, rather than unipolar (1 or 0), and causing it to modulate a fast pseudo-random bipolar binary pulse train. To recover the data it is necessary to cross-correlate the received fast binary waveform with a replica pseudo-random waveform in the correct relative phase. In such systems the fast sequence is determined under the control of a steady clock pulse train and serves effectively as a carrier in a suppressed carrier double sideband pulse-amplitude-modulated system. Changes in the data input invert the fast bit sequence but leave unchanged its phase within the repetition cycle.

With such systems, the repetition period of the code sequence is deliberately made long, with the result that the time taken to ascertain the correct phase for the replica is considerable. This imposes the loss of a correspondingly large amount of data while resynchronising after an interruption of reception.

It is an object of this invention to provide an alternative system capable of rapid synchronisation.

According to one aspect of the invention there is provided a method of increasing the bandwidth of a data signal, for transmission over a communication channel, by using the data signal in binary form to modulate a pseudo-random binary pulse train of greater bit rate than the signal, wherein the said psuedo-random pulse train is generated at least in part in response to the data signal.

According to another aspect of the invention, there is provided an apparatus for increasing the bandwidth of a data signal in binary form including means for generating a psuedo-random binary pulse train, having a greater bit rate than the data signal, at least in part in response to the data signal, and means for modulating the psuedo-random pulse train with the data signal.

According to a further aspect of the invention there is provided an apparatus for recovering an original data signal from an increased bandwidth signal generated according to the first aspect of the invention, including means arranged to derive a replica of said psuedo-random pulse train from the increased bandwidth signal and means for cross-correlating it with the increased bandwidth signal to recover said data signal.

In order that the invention may be clearly understood and readily carried into effect, examples thereof will now be described with reference to the accompanying drawings of which

*Figure 1* shows a circuit for spectrum spreading,

*Figure 2* shows a circuit for recovering the original signal

*Figure 3* is a linear equivalent of the circuit of Fig. 2, and

*Figure 4* is an alternative to the circuit of

Fig. 3.

It has been found that, for data communication, it is possible to provide spectrum spreading using sequences whose generation is repsonsive to the data input. Because of the disparity between the bit periods of the input data and the output code, in relative terms the data are static over long periods and can enter into the sequence generation logic without unduly disturbing the random properties of the resulting sequence.

The operation can be seen in an example of a simple code generator based on a 4-bit shift register implementing the recurrence equation

$$b(n) = b(n-3) \oplus b(n-4) \qquad (1)$$

Where b(n) is the value of the nth bit corresponding to the nth clock pulse and the symbol $\oplus$ represents modulo 2 addition as provided by the exclusive OR operation.

This is known to provide the repetitive 15-bit maximum length pseudo-random sequence.

----011010111100010 ----

whose power is approximately uniformly spread over its bandwidth.

If b(n) is defined instead by

$$b(n) = a(n) \oplus b(n-3) \oplus b(n-4) \qquad (2)$$

then for a(n) = 0 and the same initial conditions the same sequence will result. However, for a(n) = 1 the resulting b(n) follows the same sequence but inverted:

---- 1001010000111101 ----

This inversion holds for expessions for b(n) that contain an even number of feedback terms. Thus if a(n) is provided by the data input, which by definition is steady over many consecutive values of n, then the resulting b(n) possesses desirable spread-spectrum properties and may be taken as the output.

A suitable circuit for implementing one aspect of the invention is shown in Fig. 1. The modulo 2 addition is provided by exclusive OR gates 1 and 2 and the memory required is provided by stages $3_1$–$3_4$ of a shift register, each of which gives a delay T of one clock period. The shift register is clocked by a clock at a rate much greater than the rate of production of the data.

In the time leading up to the nth clock pulse, stages $3_1$ to $3_4$ hold binary values b(n − 1) to b(n − 4) respectively. Consequently gate 2 gives a logical output $b(n-3) \oplus b(n-4)$. To this ia added the current data value, a (n), gate 1 to give $a(n) \oplus b(n-3) \oplus b(n-4)$. This comprises modulating the fast pseudo-random pulse train $bn-3) \oplus b(n-4)$ with the data waveform a(n). When the nth clock pulse occurs, stage $3_1$ assumes this value, and all previously held values shift one stage to the right. Thus stages $3_1$ to $3_4$ now hold values b(n) to b(n − 3) respectively. It will therefore be apparent that the circuit of Fig. 1 implements equation 2 if a(n) and b(n) refer to the values obtaining just prior to the nth clock pulse.

It should be noted that, using equation 2, it is possible to choose a phase (n) in the output sequence for the inversion of the value of a(n), which will cause the shift register to contain that sequence of either all 0's or all 1's which is normally excluded. This would then be perpetuated until the next inversion of a(n). With long codes there is only a low probability of this occurring. However, logical precautions may be taken, such as holding the transition for one bit period, to prevent the occurrence of the prohibited state.

The signal b(n) is a coded data signal of bandwidth greater than the bandwidth of the data signal a(n). The signal b(n) is fed to a modulator MOD where it is modulated with an RF carrier to produce a spread spectrum signal, in a known manner; (see for example spread spectrum systems—R. C. Dixon—John Wiley & Sons). The modulation is phase shift key modulation of the carrier.

The spread spectrum signal may be demodulated in a demodulator (DEMOD) and the coded data signal fed to the circuit shown in Fig. 2.

For recovery of the data, equation 2 is modified by (modulo 2) adding $a(n) \oplus b(n)$ to each side. Since $X \oplus X = 0$ for all X this gives:

$$a(n) = b(n) \oplus b(n-3) \oplus b(n-4)$$

Thus the original a(n) can be recovered from the b sequence (apart from errors) once the shift register has been given time to fill. The is also the time for recovery of synchronisation following an interruption of the received bit stream, and is shorter than in prior art arrangements. Fig. 2 shows an implementation of equation (3) which uses the same components as Fig. 1. This circuit derives from the transmitted waveform a replica of the original psuedo-random waveform $b(n-3) \oplus b(n-4)$ and cross-correlates it with the transmitted waveform to recover the original a(n).

Circuit configurations like these of Figs. 1 and 2 have been proposed as scramblers and unscramblers in line communications applications, where it is not usually desired to increase the bandwidth occupied and the output bit rate is the same or of the same order as the data input.

(See for example Savange J. E.: Some simple Self Synchronising Digital Data Scramblers, Bell Systems Technical Journal 46 pp. 449–487 February 1967).

Thus in scrambling and unscrambling the

rate of clocking the shift register is the same or of the same order as the rate of production of the data. In these circumstances it is ensured that the signal level at the receiver is sufficient to give a low error rate in the recovered b(n) and hence of a(n). However, when the aim is to transmit a spread spectrum signal over a noisy wideband channel, the probability of making the correct binary decision for each incoming b(n) may be small. It is therefore desirable to postpone making a logical decision in this instance until operating at a lower bandwidth where the corrupting noise power has been reduced to well below the signal level.

This can be achieved by adopting linear circuits throughout for handling the combined signals and noise. Fig. 3 shows the linear equivalent of Fig. 2 in which the b(n) sequence has been made to phase shift key (PSK) modulate a coherent carrier. The modulo 2 additions are replaced by balanced modulators 4, 5 (which are linear in a restricted sense) and the shift register stages 3 are replaced by sections of a delay line 6, 7, whose delays are three bit periods and one bit period respectively. A local clock generator 8 runs with a nominal period of T. It provides an input to a further balanced modulator 9 and thus demodulates the un-delayed signal into its bipolar binary equivalent. Bandpass filters 10 and 11 remove the carrier and harmonics from the outputs of 9 and 5 while permitting the longest run of consecutive + bits (in this example 4T) to pass undistorted. The required components of the two bipolar inputs to balanced modulator 4 are coherent and provide the desired bipolar version of a(n). In contrast, interference is incoherent with the desired signals, as it is with itself when delayed, and generally is wideband. Narrow band interference gives rise to only low frequency at the output of modulator 5, and these are removed by filter 11. A lowpass filter 12 is therefore able to pass the data signal while substantially attenuating the accompanying noise power. The attenuation characteristic of filter 12 is preferably shaped in the conventional way so as to minimise inter-symbol interference. The band-limited signal then passes to a polarity detector 13 which delivers a + or − binary decision to the output.

The amplitude of the signal at the output of 12 depends on the phase of the pulses from 8 relative to the incoming bits and, in the event of their being in quadrature, is zero. Accordingly 8 must provide two quadrature outputs and the part of the circuit shown within the broken line is implemented in duplicate. Initially, one or other of the duplicates of 12 will provide sufficient output for a decision to be made in detector 13. Thereafter the phase of 12 can gradually and automatically be adjusted to optimum by a phase control 14.

As a numerical example, it will be assumed that the data rate is 20 Kb/s and is to be randomised at 20 Mb/s to give a bandwidth increase of 1000:1 or 30dB. The recurrence chosen is given by

$$b(n) = a(n) \oplus b(n-13) \oplus b(n-33)$$

whose repetition period is about 7 minutes. Then delays 6 and 7 would be 0.65 $\mu$s and 1.00 $\mu$s respectively, accurate and stable to 10 ns or less. The bandpass filters 10, 11 should pass frequencies between 150 $kH_z$ and 15 $MH_z$ and the low pass filter 12 cut off between 15 20 $KH_z$.

An alternative to filtering at the baseband is to band pass filter about the carrier frequency as shown in Fig. 4 with a narrow band filter 15 centred on the carrier frequency. The output of 15 gives a carrier signal which is quasi continuous in phase, being PSK modulated at the bit rate of the data and accordingly occupies only a narrow bandwidth. By contrast, any interference power at the output of modulator 4 is wideband and is strongly attenuated by filter 15. If desired, the narrowband filtering can be executed at a lower frequency by means of heteodyning, preferably with the local oscillator at a sub-multiple of the carrier. Clock and bit recovery from the PSK waveform can then be performed in the conventional way. Where the heterodyne technique is adopted, the phase of the local oscillator could, with advantage, be continuously optimised. It should be noted that the delay of 6 should here be made less than nominal to allow for the group delay of 11.

## CLAIMS

1. Apparatus for increasing the bandwidth of a data signal in binary form, including
means for generating a psuedo-random binary pulse train, having a greater bit rate than the data signal, at least in part in response to the data signal, and
means for modulatng the pseudo-random pulse train with the data signal to produce an increased bandwith signal.

2. Apparatus according to claim 1, wherein the means for generating a pseudo-random binary pulse train comprises a delay means, and means for producing, as said train, a combination of signals subjected to different delays in the delay means and the modulating means comprises an input for receiving the said data signal, a further input coupled to receive the said combination thereby to modulate the combination with the data signal to produce the increased bandwidth signal, and an output coupled to the delay means to deliver thereto the modulated combination.

3. Apparatus according to claim 2, wherein the delay means comprises a shift register having a plurality of stages and a clock for

clocking the shift register at a rate greater than the bit rate of the data signal and the combination producing means is connected to combine the outputs of different stages of the register.

4. Apparatus according to claim 2 or 3, wherein the combination producing means comprises at least one adder.

5. Apparatus according to claim 2, 3 or 4 wherein the combination producing means comprises at least one Exclusive-OR gate.

6. Apparatus according to claim 1, 2, 3, 4 or 5 wherein the modulating means comprises an adder.

7. Apparatus according to claim 6 wherein the modulating means comprises an Exclusive-OR gate.

8. Apparatus according to any preceding claim, in combination with means for modulating a radio frequency carrier with the increased bandwidth signal to produce a spread-spectrum signal.

9. A method of increasing the bandwidth of a data signal, for transmission over a communication channel, by using the data signal in binary form to modulate a pseudo-random binary pulse train of greater bit rate than the signal, wherein the said psuedo-random pulse train is generated at least in part in response to the data signal.

10. Apparatus for recovering an original data signal from an increased bandwidth signal generated according to the method of claim 9 or by the apparatus of anyone of claims 1 to 8, including means arranged to derive a re-plica of said psuedo-random pulse train from the increased bandwidth signal, and means for cross-correlating it with the increased bandwidth signal to recover the said data signal.

11. Apparatus according to claim 10, wherein the replica deriving means includes a delay means arranged to receive the increased bandwidth signal and means for producing, as the said replica, a combination of signals subject to different delays in the delay means, and the cross-correlating means comprises an input for receiving the increased bandwidth signal, a further input coupled to receive the combination, thereby to cross-correlate the replica and the increased bandwidth signal, and an output of the original data signal produced by the cross-correlation.

12. Apparatus according to claim 11, wherein the delay means comprises a shift register having a plurality of stages and a clock for clocking the shift register at the bit rate of the increased bandwidth signal, and the combination producing means is connected to combine the outputs of different stages of the register.

13. Apparatus according to claim 11 or 12, wherein the combination producing means comprises at least one adder.

14. Apparatus according to claim 10, 11, 12 or 13 wherein the cross-correlating means comprises an adder.

15. Apparatus according to claim 11, for recovering an original data signal from an increased bandwidth signal modulated on an RF carrier, wherein the delay means includes delay line sections, the combination producing means comprises at least one balanced modulator connected to combine the outputs of different ones of the sections, and the cross-correlating means comprises a balanced modulator.

16. Apparatus according to claim 15, further including a band pass filter connected to receive the said combination and pass it to the cross-correlating means, whilst removing the carrier and its harmonics.

17. Apparatus according to claim 15 or 16, further including a narrow band filter, centred on the carrier frequency, connected to receive the output of the cross-correlating means.

18. Apparatus according to claim 15 or 16, further including demodulating means for receiving the increased bandwidth signal modulated on the carrier, the cross-correlating means being coupled to the demodulating means to receive therefrom the increased bandwidth signal.

19. Apparatus according to claim 19 wherein the demodulating means includes a local clock generator and a balanced modulator.

20. Apparatus according to claim 20, wherein the cross-correlating means is coupled to the balanced modulators by a band pass filter for removing the carrier frequency and its harmonics.

21. A method or apparatus for increasing the bandwidth of a data signal in binary form substantially as hereinbefore described with reference to Fig. 1 of the accompanying drawing.

22. Apparatus for recovering an original data signal from an increased bandwidth signal substantially as herein before described with reference to Figs. 2, 3 or 4 of the accompanying drawing.

Printed for Her Majesty's Stationery Office
by Burgess & Son (Abingdon) Ltd.—1979.
Published at The Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.

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